FIG. 1

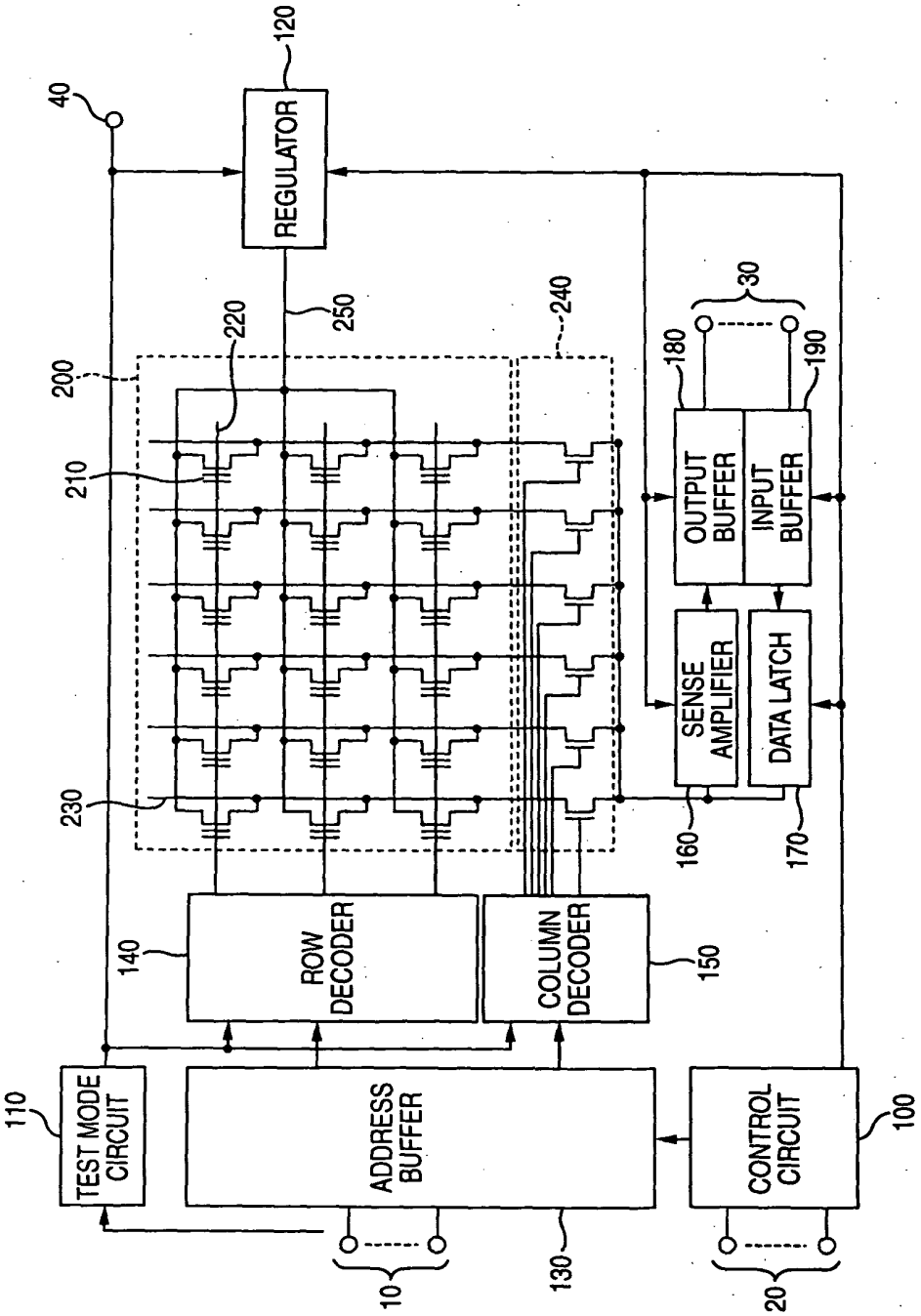

REGULATOR
120
40
250
240
220
200
210
230
30
180
190
OUTPUT BUFFER
INPUT BUFFER
SENSE AMPLIFIER
DATA LATCH
160
170
ROW DECODER
140
COLUMN DECODER
150
TEST MODE CIRCUIT
110
ADDRESS BUFFER
130
CONTROL CIRCUIT
100
10
20

FIG. 2

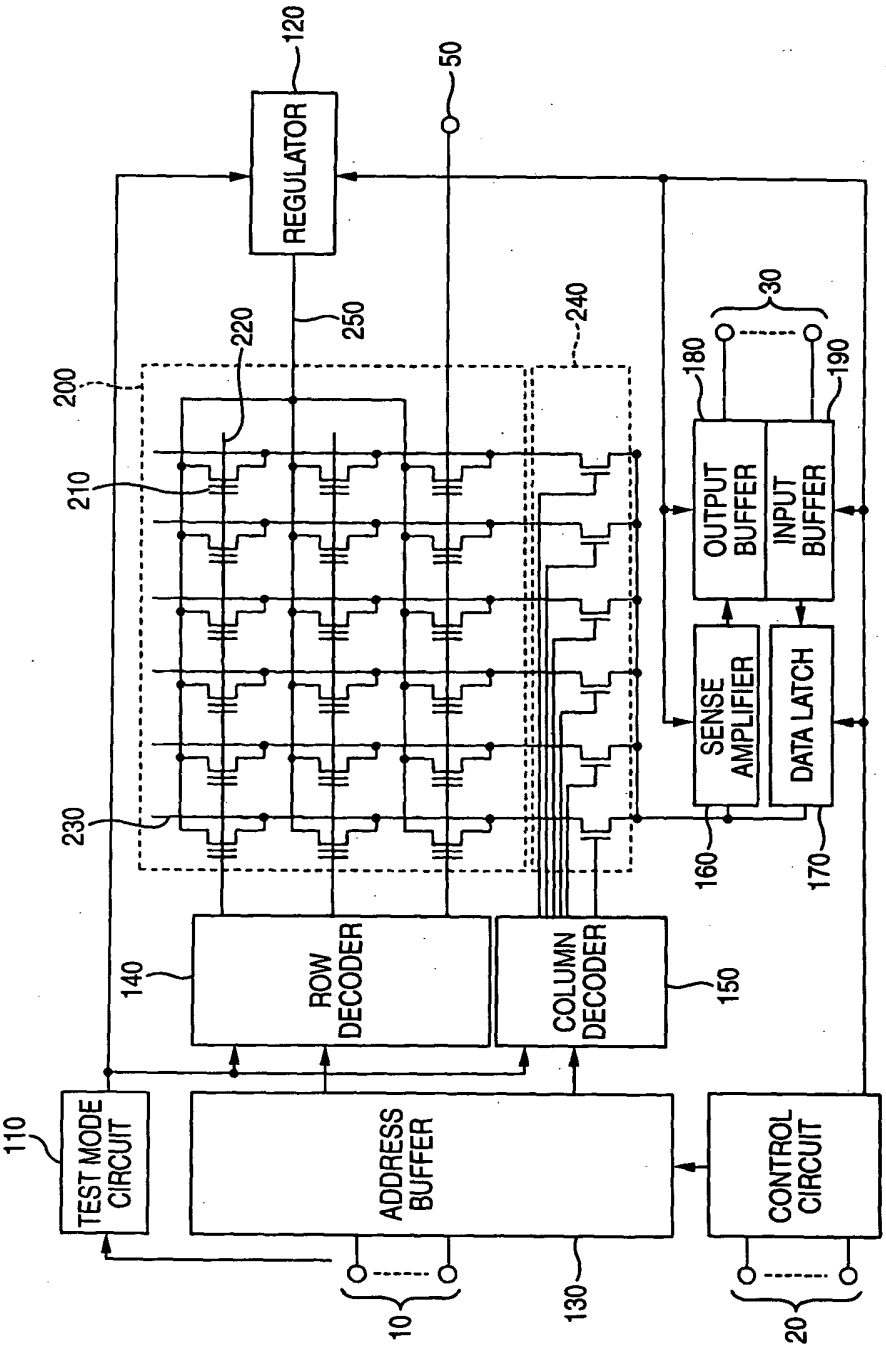

REGULATOR
120
50
200
210
220
230
240
250
30
180
190
OUTPUT BUFFER
INPUT BUFFER
SENSE AMPLIFIER
DATA LATCH
160
170
ROW DECODER
140
COLUMN DECODER
150
TEST MODE CIRCUIT
110
ADDRESS BUFFER
CONTROL CIRCUIT
10
130
20

FIG. 3

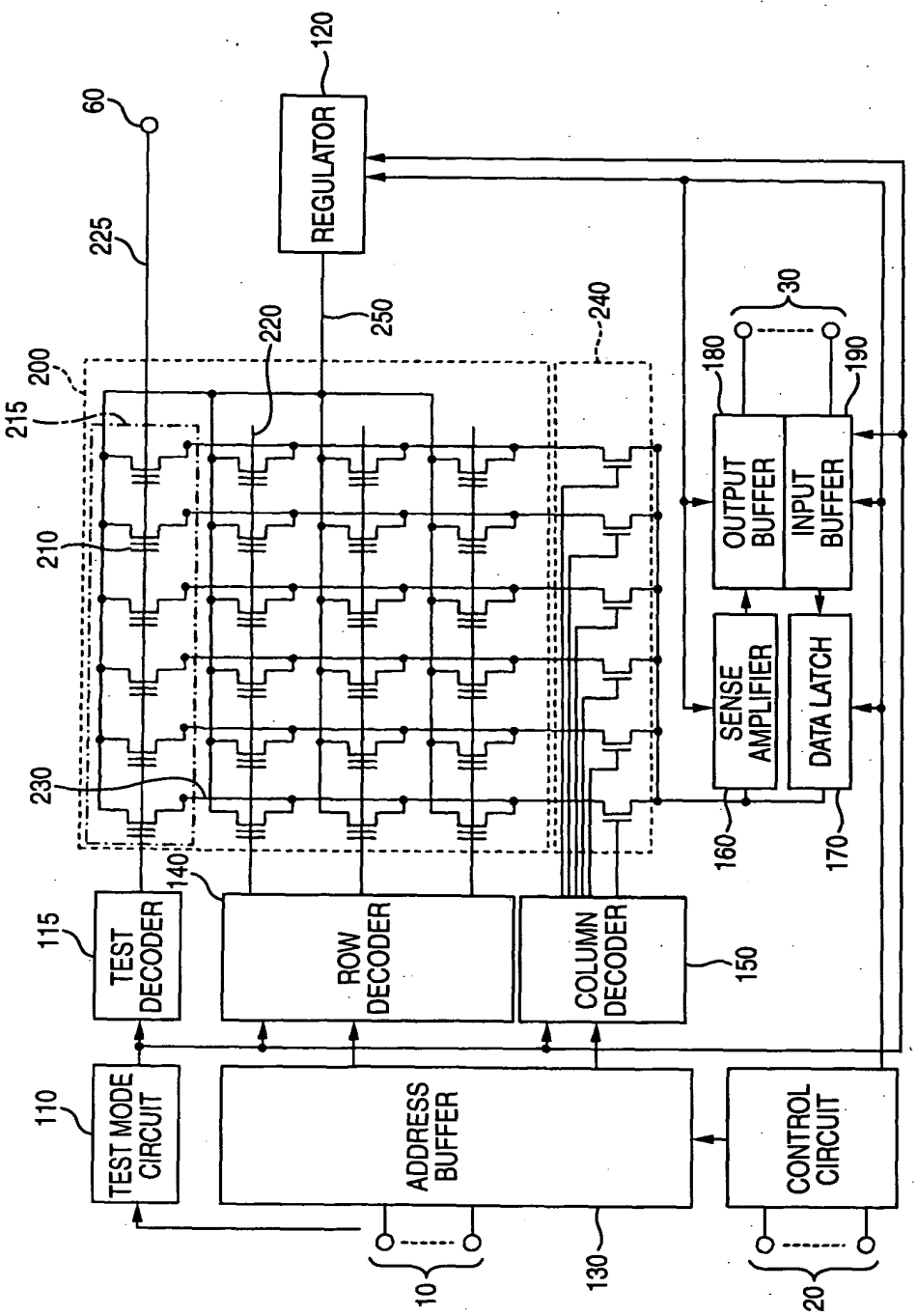
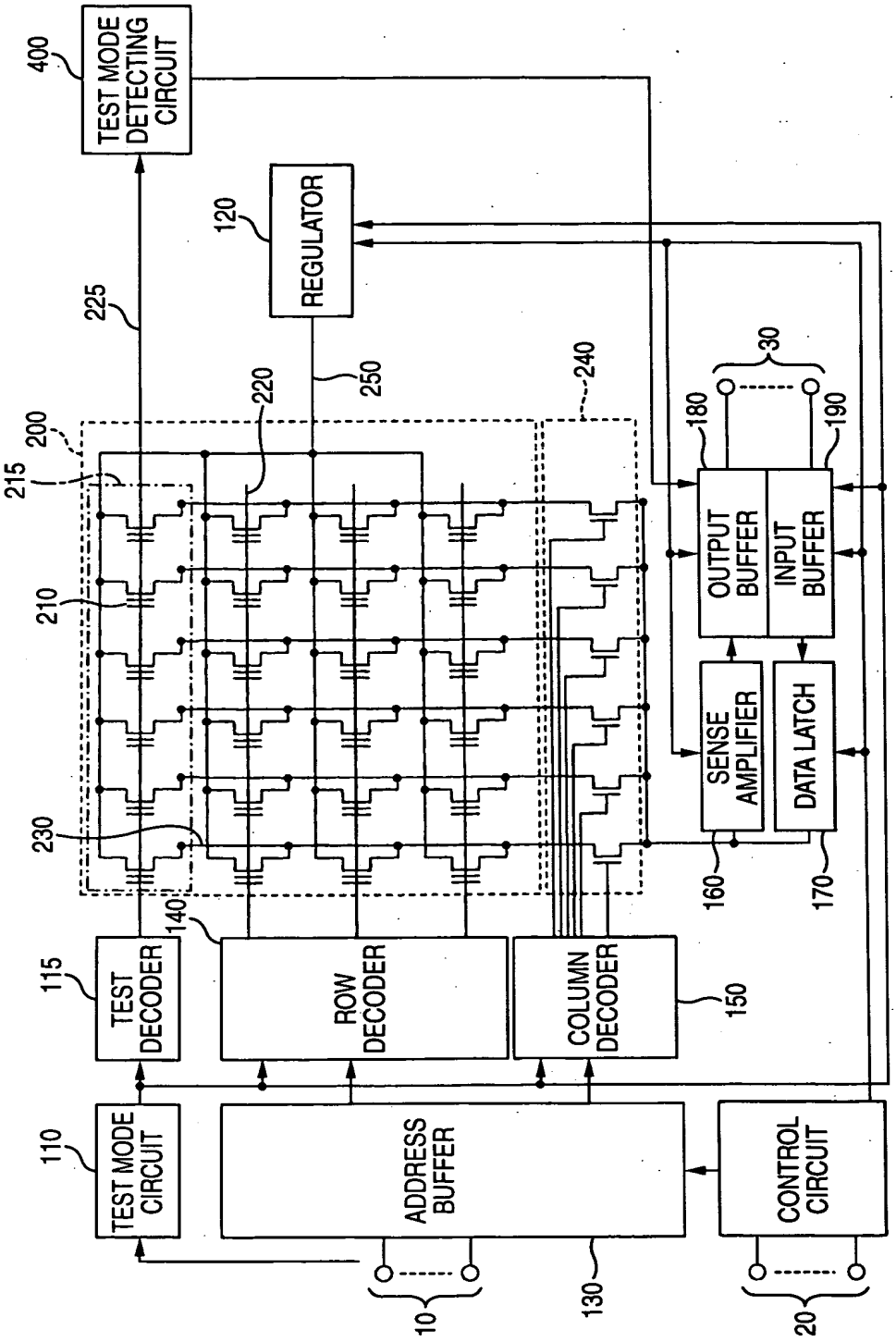

REGULATOR
120
60
225
250
240
220
200
215
210
230
30
180
190
OUTPUT BUFFER
INPUT BUFFER
SENSE AMPLIFIER
DATA LATCH
160
170
TEST DECODER
115
140
ROW DECODER
COLUMN DECODER
150
TEST MODE CIRCUIT
110
ADDRESS BUFFER
CONTROL CIRCUIT
10
130
20

FIG. 4


400
TEST MODE DETECTING CIRCUIT
120
REGULATOR
225
250
220
240
30
180
190
200
215
210
230
OUTPUT BUFFER
INPUT BUFFER
SENSE AMPLIFIER
DATA LATCH
160
170
140
115
TEST DECODER
ROW DECODER
COLUMN DECODER
150
110
TEST MODE CIRCUIT
ADDRESS BUFFER
CONTROL CIRCUIT
10
130
20